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Implementation of ASDM scheme for Current Mode Inverter

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Abstract:

The objective of this paper is to simulate a current mode asynchronous sigma-delta modulation (CASDM) control scheme for inverters application. The CASDM has the advantage of circuit simplicity and low harmonic components which is good for grid-tied inverter application. The major contribution of this paper includes simulation of the CASDM control scheme using MATLAB and applying it to the grid-tied inverter successfully. It can be noted here CASDM can be very useful for other power electronics applications such as the reactive power feeding inverters connected to grid, active power line conditioner, and current-controlled motor driver also. In this paper, CASDM operation principle will be introduced and mathematical expression of the controller will be derived. Finally, computer simulations and performance results are discussed.

Keywords— **Asynchronous sigma delta modulation; Grid tied Inverter; MATLAB Simulation.**

I. INTRODUCTION

The requirement of modern age is to use the non-renewable energy effectively and efficiently. There are many ways to utilize this potential energy like solar energy by directly feeding into grid without use of storage and batteries. It also reduces the number of power conversions. For this kind of applications grid tied inverters can be use. At the same time this inverters can be useful for reactive power feeders. To fulfill this task, usually, a full-bridge inverter is adopted to realize the grid-tied power generation system [1-2]. The grid-tied inverter needs to inject a sinusoidal current into the ac mains; in such applications current-mode control is required [3-4]. The sinusoidal pulse width modulation (SPWM) is the most used control strategy for the inverter [5-6]. Recently, the sigma delta modulation (SDM) is getting popular in various applications of power electronics because of its circuit simplicity, fast response, and low harmonics [7-8]. In addition to these advantages the asynchronous SDM (ASDM) can be implemented without the synchronization clock is also a promising control method for various types of power converters [9-10]. Though, it is still not a common control method for power converters.

II. THE ASDM SCHEME AND CIRCUIT

In 1962 Sigma Delta Modulation technique was proposed. It overcomes the major drawback of transmitting DC components in the delta modulation. Due to the reason of high noise immunity SDM has very good performance on the analog-to-digital conversion. Therefore the SDM has been applied to the field of communication for a long time. As rapidly developed power electronics technology, the SDM has been used for power converter control successfully [11-14]. Further ASDM simplifies the circuitry of the SDM and can be easily implemented by using analog components. Also there is no need of synchronization clock. It is not a very common modulation scheme. The ASDM has the advantages of circuit simplicity and low harmonics components which make it very attractive for power electronics applications.

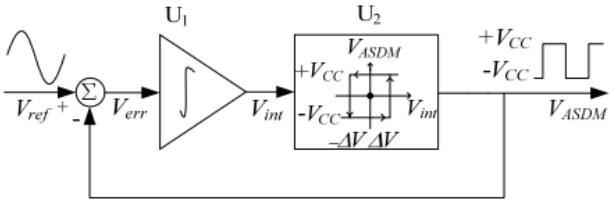

Fig.1 ASDM block diagram

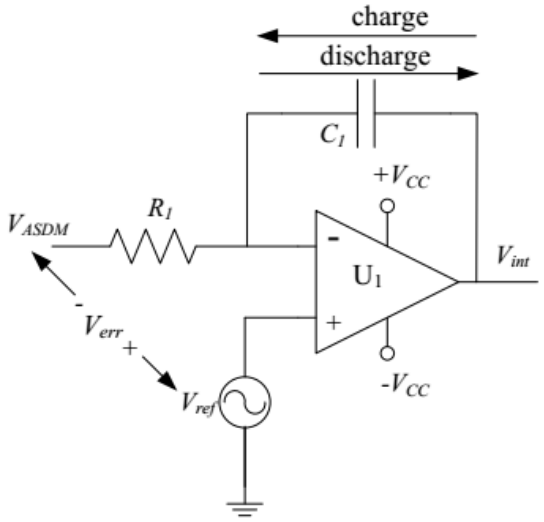

Fig. 2(a) Typical ASDM Circuit Implementation

A. *ASDM CIRCUIT IMPLEMENTATION*

As shown in Fig. 1 block diagram of the ASDM, consists of three major blocks in ASDM , an integrator with error amplifier, U1, and a hysteresis comparator, U2 and a feedback summing point. The difference (Delta) between the input reference, Vref, and the output pulsating voltage train, i.e. the error signal, Verr, is applied as feedback to the integrator. The integrated signal, Vint, is the accumulated (Sigma) error signal which will be processed by the comparator to generate the output pulsating voltage train, VASDM, which can be applied to the power switches in the power converter to regulate the electric power flow. Fig. 2 (a) shows the typical circuit of integrator implementation of inside the ASDM and the corresponding key waveforms are shown in Fig. 2(b). One point must be noted here modulating frequency should be higher than the Nyquist rate so as to achieve the sustained oscillations.

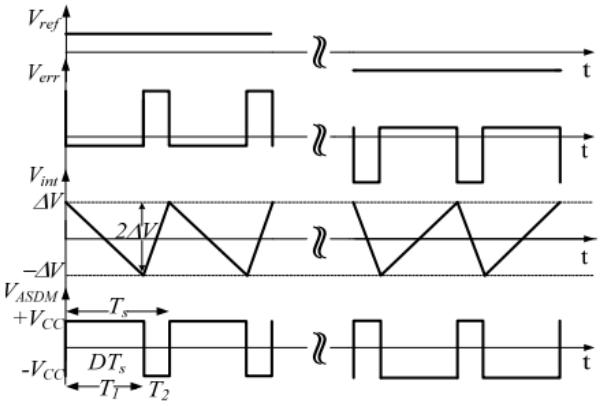

Fig. 2(b) Key waveforms

III. MATHEMATICAL DERIVATIONS

The output of the Hysteresis is either positive or negative, oscillating between the +Vcc and –Vcc. As shown in fig2(a), this feedback is given to integrator therefore the output of integrator is either positive going ramp or negative. As in Fig. 2(b), during the time period T1 when Verr is a negative constant, the integral signal Vint will decrease with a negative slope, Sint-, which can be expressed as:

$$S_{int}- = \frac{V_{ref} - V_{cc}}{\tau} \qquad (1)$$

Where $\tau = R1C1$ is the time constant of the integrator.

From(1),the time period T1 can be expressed as :

$$T_1 = \frac{-2\Delta V}{S_{int}-} \qquad (2)$$

When the Vint with a positive slope reaches the upper boundary of the hysteresis band, ΔV, the value of VASDM will be altered again from -Vcc into +Vcc and a switching cycle is completed.

$$S_{int}+= \frac{V_{ref} + V_{cc}}{\tau} \qquad (3)$$

$$T_2 = \frac{2\Delta V}{S_{int}+} \qquad (4)$$

From (2) and (4), the duty ratio, D, and the switching frequency, fs, of the ASDM can be determined as:

$$D = \frac{1}{2} + \frac{V_{ref}}{2V_{cc}} \quad (5)$$

Where VCC is the DC rail voltage of the op-amps, V is the hysteresis voltage window of the band-band comparator, and is the time constant of the integrator.

$$f_s = \frac{{V_{cc}}^2 - {V_{ref}}^2}{4\tau \Delta V V_{cc}} \quad (6)$$

Equation (6) shows that the ASDM has various switching frequencies which can spread switching noise over a broader frequency spectrum. It has the benefit of low electromagnetic interference. Also, the switching frequency is affected by several variables including Vref, ΔV, and τ. In order to control the switching frequency under moderate scale, the magnitude of ΔV and τ must be carefully selected.

For inverter applications, the reference signal can be assumed to be a constant value during a switching period since the reference voltage frequency is much smaller than the switching frequency. Equation (5) shows that the duty ratio of the PWM control signal is linearly proportional to the reference signal and is irrelevant to the circuit parameters, such as ΔV or τ. It implies that the ASDM can achieve very good controllability

IV. GRID-TIED INVERTER USING ASDM

For grid-tied inverter, the output current must be sinusoidal and synchronized with the AC mains voltage. Several current control strategies, such as the hysteresis current control or the predictive current control, have been promoted to control the inverter's output current. The ASDM is also capable of regulating the output current of the grid-tied inverter. The circuit diagram of a conventional grid-tied full-bridge the inverter is shown in Fig. 3.

Assuming the power switches are operated in the bipolar-switching modewhich means that the voltage potential across terminalA and B, vab(t), is either +VDC or –VDC. Therefore, the effective voltage, vab,eff(t), developed on terminal A and B over one switching period is resolved by the duty ratio and can be expressed as:

$$V_{ab,eff}(t) = \frac{1}{T_S}\left[\int_0^{DT_S} V_{DC}\,dt + \int_{DT_S}^{T_S} (-V_{DC})dt\right] \quad (7)$$

$$= (2D(t) - 1)V_{DC} \quad (8)$$

where D(t) is the duty ratio shown in time-varying format. For the inverter application, the reference signal, vref(t), is a sinusoidal function and (5) can be rewritten as Combining (7) and (8), the effective voltage, vab,eff(t), can be expressed as:

$$V_{ab,eff}(t) - V_{ac}(t) = L\frac{di_{ac}(t)}{dt} \quad (9)$$

where L is the inductance of the inverter output inductor.

$$\frac{\frac{V_{DC}}{V_{CC}}.\bar{V}_{ref}(t) - \bar{V}_{ac}}{j\omega L} = \bar{\imath}_{ac} \quad (10)$$

Equation (10) explains that vab,eff(t) is also a sinusoidal function because of the sinusoidal control signal, vref(t).

As shown in Fig. 3, the output current of the inverter, iac(t), is equal to the inductor current which can be resolved by the effective terminal voltage, vab, eff(t), and the AC mains voltage, vac(t). That is:

It should be noticed that both vab,eff(t) and vac(t) in (10) are time domain sinusoidal function with the equal frequency. Therefore, (10) can be expressed in complex number format for steady state analysis.

By combining (9) and (10), the following steady-state current expression in a complex number the format can be obtained:

$$\left|\bar{V}_{ref}\right| = \frac{V_{CC}}{V_{DC}}\left(|V_{ac}|^2 + \omega^2 L^2 \left|\bar{\imath}_{ac,ref}\right|^2\right)^{\frac{1}{2}} \quad (11)$$

$$\angle\theta_{ref} = \tan^{-1}\left(\frac{\omega L\left|\bar{\imath}_{ac,ref}\right|\cos\theta_i}{|V_{ac}|}\right) \quad (12)$$

Where ω is the angular frequency of the AC mains and variables with arrows on the top are shown in phasor forms. Equation (11) exhibits that the output current of the inverter is decided by the reference signal because other variables in (11) are constants or the fixed AC mains voltage. It require considering that the injected AC line current produced by the

Grid-tied inverter should be in phase with the AC mains voltage. Therefore, the reference signal for the grid-tied inverter should never be in phase with the AC mains voltage because of the imaginary term in the denominator of (12). In order to obtain the desired output current, the reference signal of the CASDM needs to be carefully decided from (11), the amplitude and phase angle of the reference the signal for the CASDM controlled grid-tied inverter with desired output current can be expressed as:

It should be noticed that (11) and (12) are obtained under the steady-state analysis, once the reference signal for the CASDM has been solved.

On the other hand, the reference signal, vref, is produced by the reference signal generator based on

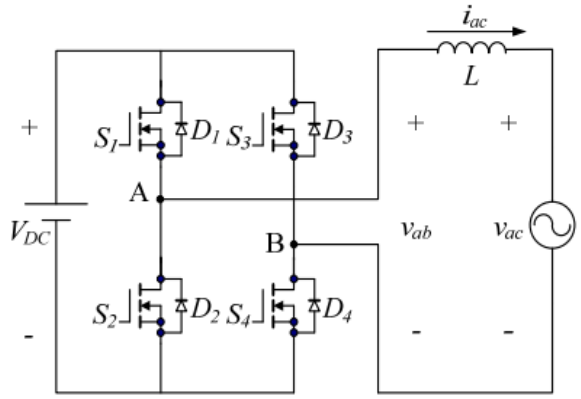

Fig. 3. Typical Grid-Tied Inverter

the derived equations (11) and (12) with quantities of VDC, vac, and iac,ref. The reference signal and the current error signal are sent into the reference current generator to generate the desired reference signal, vref, for the ASDM. Then, the ASDM will generate the gate signals, vGS1~vGS4, for the power switches of the grid-tied inverter. With the appropriate gate signals, the desired sinusoidal current will be injected into the AC mains.

V. MATLAB SIMULATIONS AND RESULTS

The performance of ASDM for power electronics switching devices can be investigated using modeling and simulation software like MATLAB; fig. 5 shows the common implementation using integrator and hysteresis. ASDM scheme can be successfully used for generating the gate pulses required by GTI (Grid-tied Inverter) fig. 4 shows the MATLAB modeling of GTI. Full bridge inverter can be used in current mode. Grid tied inverter need to produce the necessary current in phase with the voltage. As shown in (9) the value of current depends on the difference between grid voltage & inverter output and value of inductor, so it must be resolved correctly.

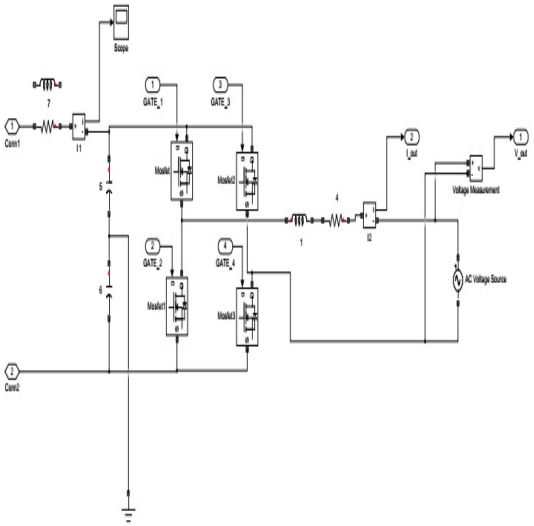

Fig. 4. Grid-Tied InverterModeling in MATLAB

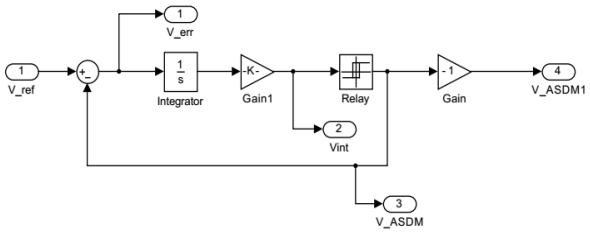

Fig. 5. MATLAB modelling for ASDM

On the basis of obtained equations for the CASDM, MATLAB simulations results are shown to validate the performance of the grid-tied inverter. In the following simulation, the dc rail voltage, VCC, is 15V, the hysteresis bandwidth, ΔV, is set

to be 0.5V while the time constant, τ, is equal to 0.1ms. Fig. 6 shows the significant waveforms of the CASDM with reference signal +10V. From (5) and (6) with a +10V reference signal, the calculated duty ratio is 0.83 and the calculated switching frequency is about 41.7 kHz. As shown in Fig. 5 (a) with Vref =+10 V, the simulated duty ratio is 0.83 and the simulated switching frequency is about 41.7 kHz. Similarly, when the reference signal becomes -10V, the simulated duty ratios, as shown in Fig. 5, agrees with the calculated one, which is 0.17. Also, the simulated switching frequency is shown in Fig. 5 is about 41.7 kHz which also agree with the calculated one.

By following the design procedure proposed in this paper, the output current of the grid-tied inverter can be well controlled. The computer simulations of the grid-tied inverter with the proposed CASDM controller for 3 A (Im) output currents are shown in Fig. 6, shows the fixed grid voltage considered as 110V (Vm),Vdc at inverter is chosen as 200V, greater than grid voltage, output current and sinusoidal reference voltage which agrees with calculation. It can be observed that the almost sinusoidal current with desired amplitude can be generated. Also, the power factor (PF) at the AC mains is almost unity.

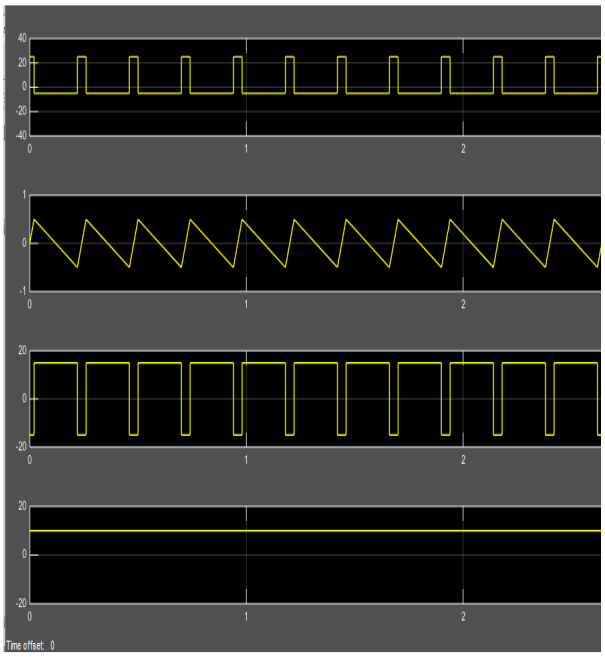

Fig. 5 (a). Key Waveformsi) Verr ii) Vint iii) VASDM iv) Vref = +10v

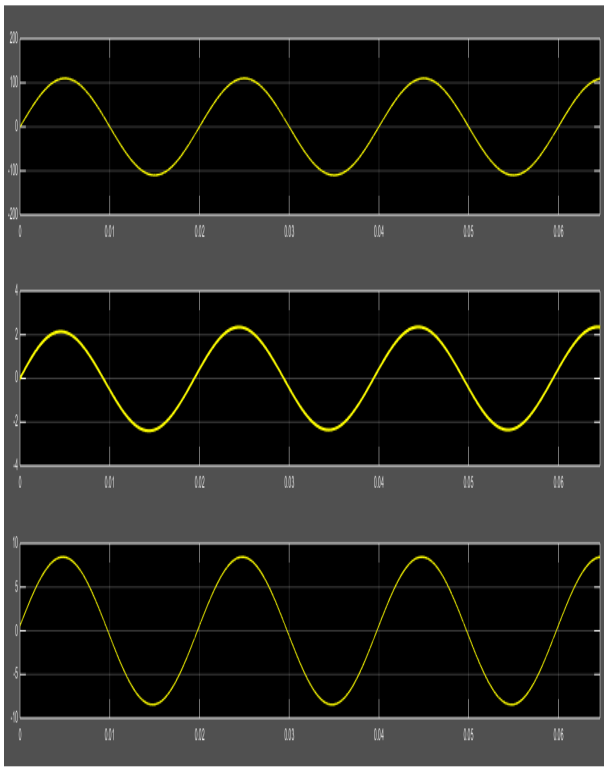

Fig.6. i) Grid voltageii) Output Current, Im iii) Vref

VI. CONCLUSIONS

In this paper, the CASDM for the grid-tied inverter is described. The operation principle of the proposed CASDM is introduced. The derivation of the reference signal and the feedback control strategy for the proposed CASDM is presented. Computer simulations and results are shown to verify the performance of the grid-tied inverter with the proposed CASDM.

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